RADIO CORPORATION OF AMERICA
SEMICONDUCTOR AND MATERIALS DIVISION
SOMERVILLE, N. J.

QUARTERLY REPORT NO. 2

for

GALLIUM ARSENIDE VARACTOR DIODES

THIS REPORT COVERS THE PERIOD

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ABSTRACT

During this quarter, emphasis was placed on improving cutoff frequencies of devices having breakdown voltages in excess of 14 volts. In addition to the use of epitaxial material, techniques were developed for mechanically controlling the thickness of the base region of the diodes. This approach has yielded substantial improvements in diode cutoff frequency.

PART I

I. PURPOSE

The purpose of this contract is to develop a series of gallium arsenide varactor diodes capable of yielding forty percent (40%) power conversion efficiency from 12 Gc to 24 Gc. Phase II of this contract is to develop a device that is able to meet the following circuit objectives:

(a) Input frequency of 12 Gc

(b) Output frequency of 24 Gc

(c) Input power of 100 mw

(d) Output power equal to or greater than 40 mw at 25°C

A total of ten units will be submitted to the Contracting Agency, together with all required reports.

II. TECHNICAL DISCUSSION

A. Device Specification

In the first quarterly report of this contract, expressions were derived for the power handling capability and conversion efficiency of a varactor diode. The maximum power input for optimum efficiency was shown to be:

$$P_{in} = \frac{1}{35} \omega \, C_{min} \, (\phi + V_B)^2 \; \ldots \ldots \ldots \ldots \ldots \ldots \ldots \quad (1)$$

where:

ω = input angular frequency

C_{min} = minimum junction capacitance

V_B = breakdown voltage

ϕ = built-in potential (1 volt for Gallium Arsenide)

Figure (1) shows the relationship between V_B and C_{min} which must be satisfied at 12 Gc for an input power level of 100 mw in order to obtain optimum conversion efficiency.

The conversion efficiency was shown to be determined by the ratio

$$\frac{f_{in}}{f_{c\,(max)}}$$

where:

f_{in} = input frequency, $f_{c\,(max)} = \dfrac{1}{2\pi R C_{min}}$

R = diode series resistance

The impedance level of the circuit, was not considered in the derivation of Equation (1). It cannot, however, be neglected in practice. It is desirable to have the dynamic diode resistance at the input frequency much higher than the diode series resistance. C_{min} should therefore, be

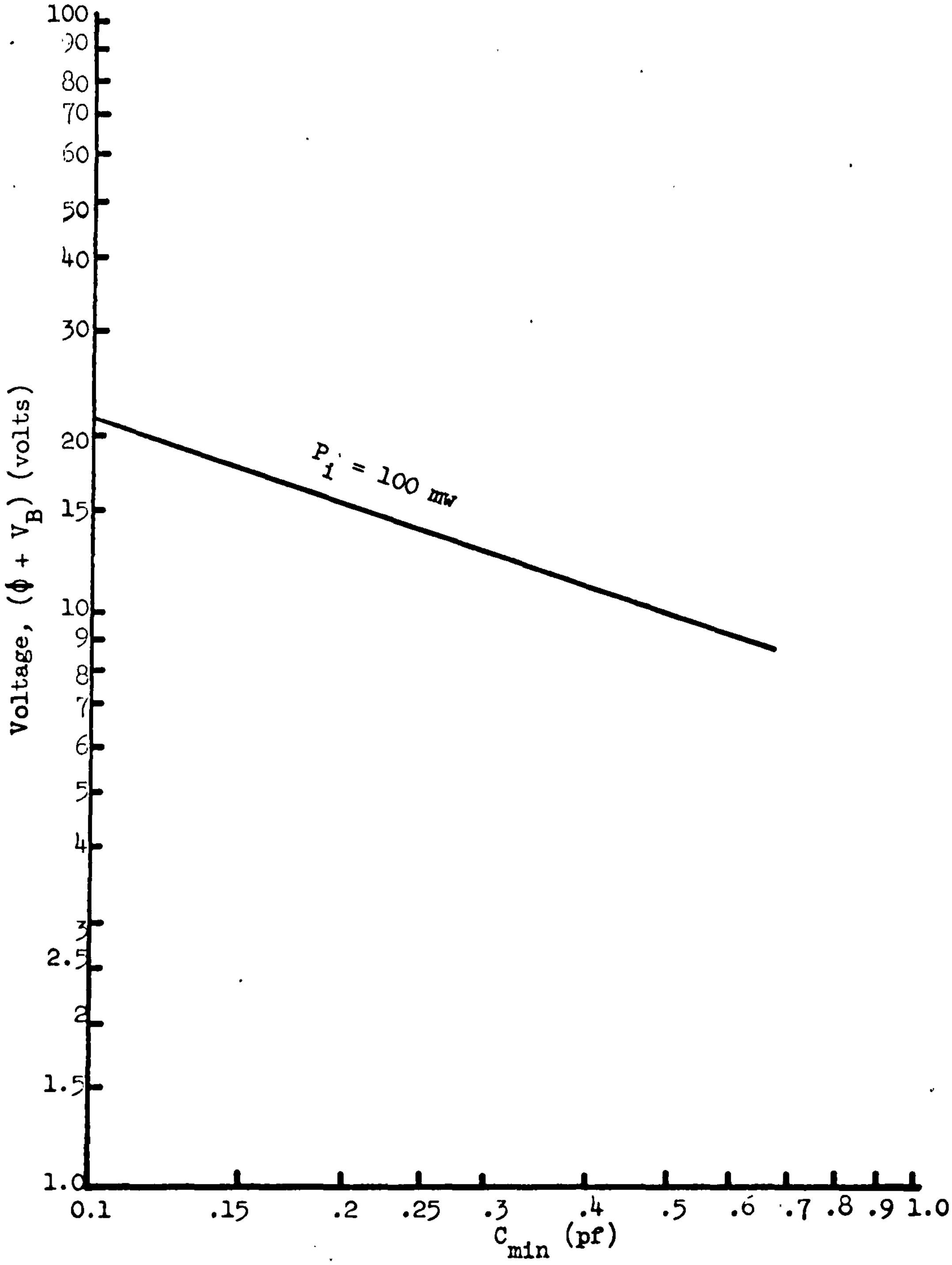


FIGURE 1 BREAKDOWN VOLTAGE vs. MINIMUM CAPACITANCE FOR 100 mw DIODE INPUT POWER AT 12 GC (BEST CONVERSION EFFICIENCY)

made as small as possible commensurate with power handling and power dissipation requirements.

To obtain 40% conversion efficiency, $\frac{f_{in}}{f_{c\,(max)}}$ must be equal to or less than 0.050. At 12 Gc input frequency, $f_{c(max)}$ must therefore, be greater than 240 Gc.

B. Device Design

1. Very Thin and Well Structures

In the first report, it was shown that the use of epitaxial material offered the simplest means of producing high cutoff diodes. Serious technical difficulties still exist at this time, however, in controlling the characteristics of Gallium Arsenide epitaxial layers. An alternate approach to the use of epitaxial material is being investigated which consists in mechanically reducing the thickness of the base region directly under the junction.

Figure (2) is a plot of the resistance of the diode base region as a function of the base thickness, for two values of junction diameters. These values were obtained using the published solutions of the Laplace equation with appropriate boundary conditions. (D.P. Kennedy, J.A.P. Vol. 31, p. 1440, 1960).

It is evident that the resistance decreases most rapidly when the base thickness is under about one mil. When the resistance of the diffused region and of the contacts is minimized, substantial improvements in diode cutoff frequency are possible if very close control of the base thickness can be achieved. Attempts were made to lap or etch down pellets to a total thickness of about one mil. A number of excellent devices were produced in this manner, but yields were generally poor.

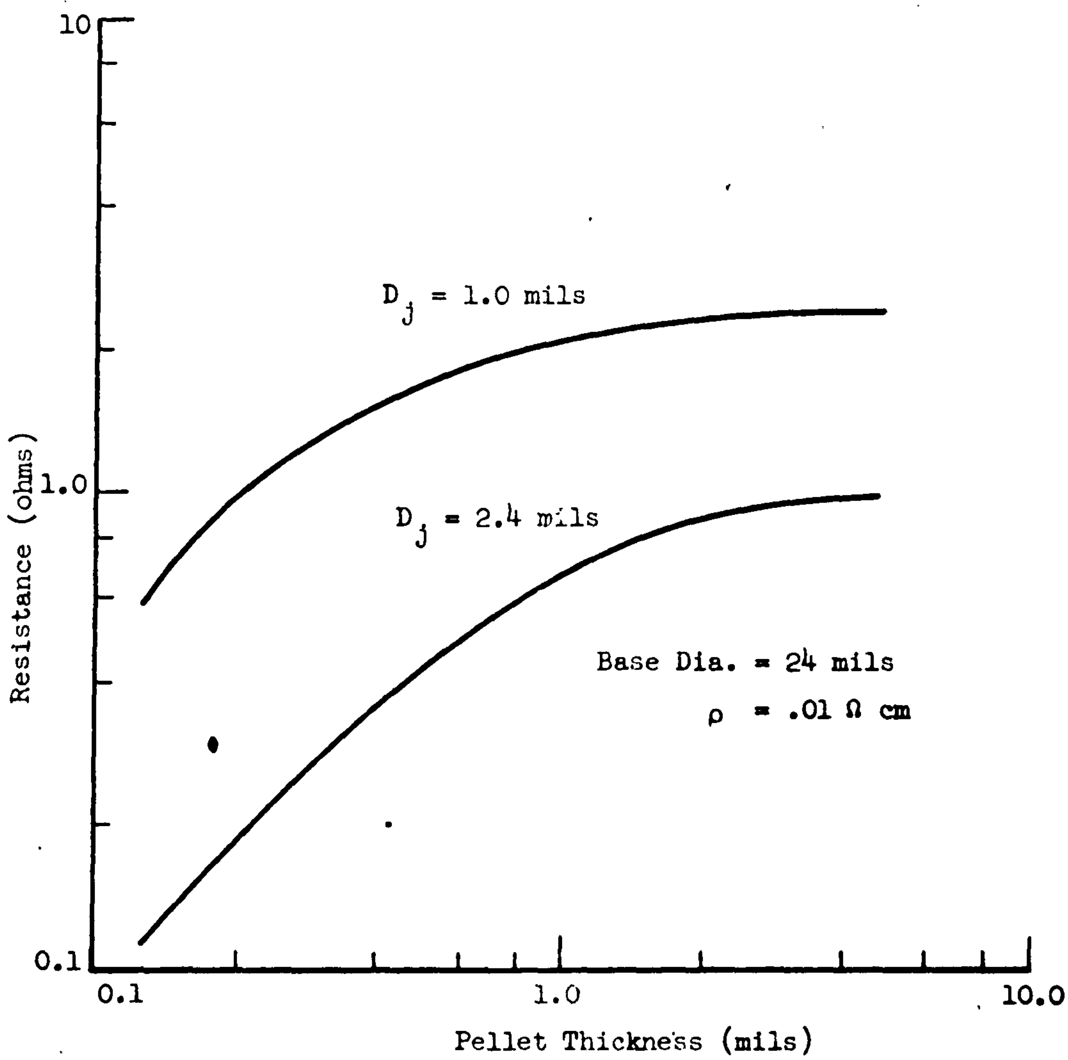


FIGURE 2 RESISTANCE VS. PELLET THICKNESS FOR TWO JUNCTION DIAMETERS, D_j

Most of the pellets crumbled during processing or were broken during alloying to the package.

The characteristics of the best very thin units fabricated this quarter are shown in Table I. The improvement of the lowest voltage

TABLE I

CHARACTERISTICS OF VERY THIN DIODES

C_{jo}	V_B	f_c (at V_B)§
0.647	13	330
0.365	32	390
0.636	30	380
0.412	34	360

§Extrapolated from cutofff frequency measured at -6 volts and 10 kmc/s

units (13 volts) was relatively small with thin base structures. This is to be expected since the ratio of junction radius to pellet radius is smaller than for devices made from lower resistivity material for a given value of capacitance. Figure (2) also shows that in order to bring about an appreciable resistance reduction in a one mil diameter junction, the base must be substantially thinner than for a 2.4 mil diameter unit.

An alternate approach has, therefore, been tried which consists of placing the junction either at the bottom of a well, etched to the desired depth on the wafer, or to etch a well on the reverse side of the wafer under the junction. With these techniques, the pellet is mechanically rugged since most of it is several mils thick, while the thickness of the base region under the junction may be closely controlled. Figure (3) is a drawing of the cross section of such a structure. The device is fabricated in the following manner as outlined

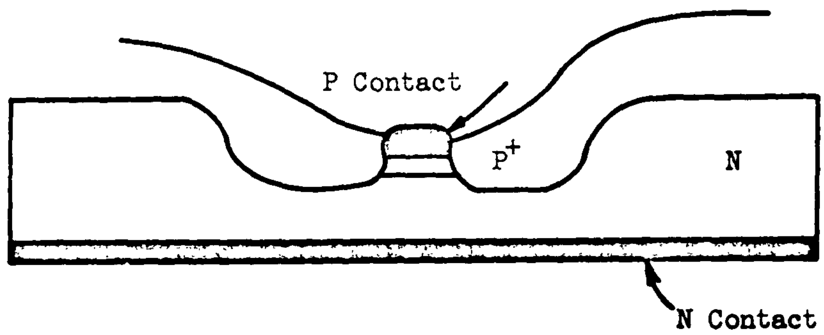


FIGURE 3 WELL STRUCTURE CROSS SECTION

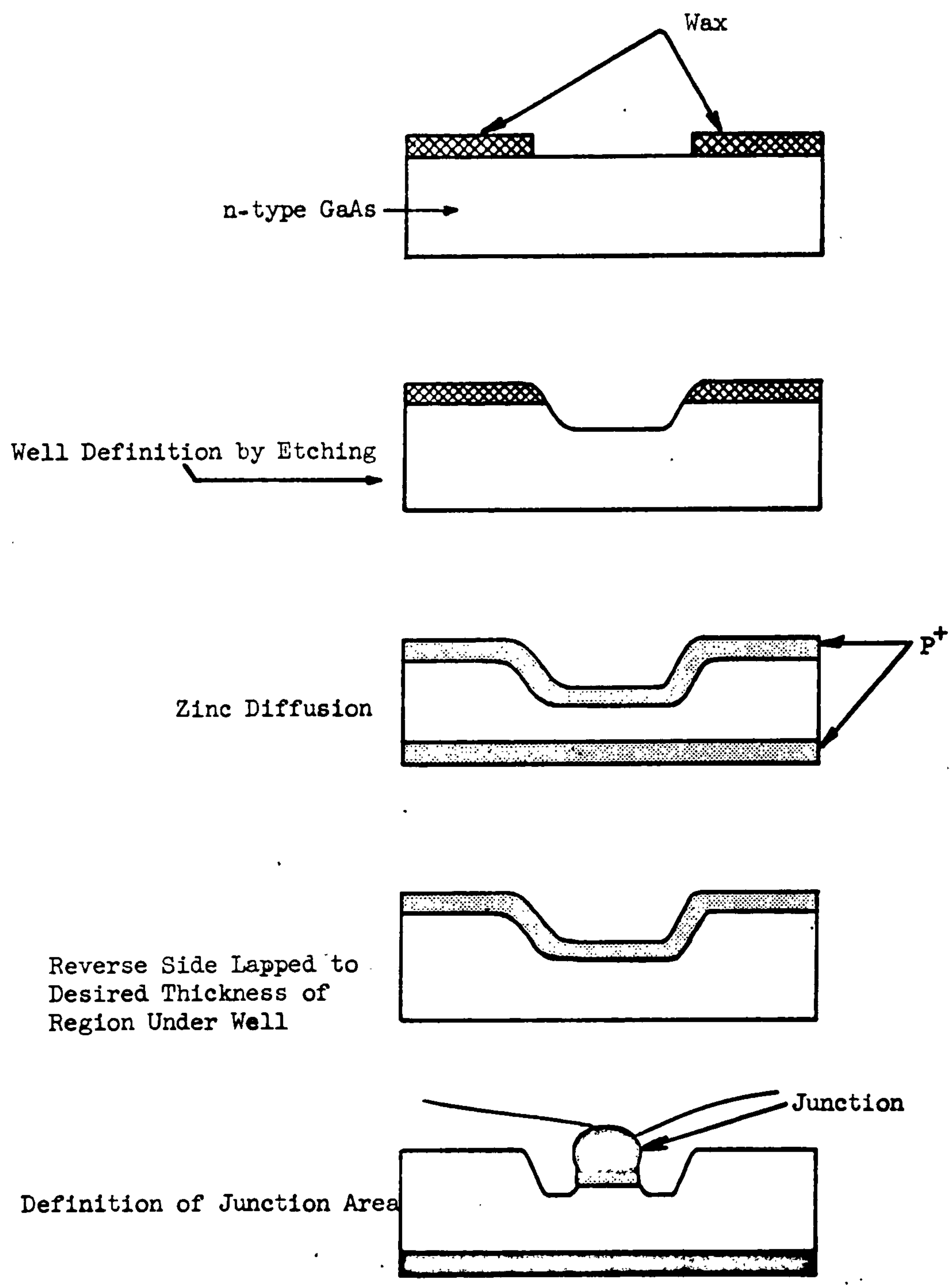


FIGURE 4 PROCESS OUTLINE FOR WELL UNITS

in Figure (4).

1. The wafer is masked with wax, except for the desired well area.
2. The wafer is etched in aqua regia until the well is defined (about 1.5 mils deep). The wax is then cleaned off.
3. The wafer is diffused.
4. The back of the wafer is lapped down until the distance between the junction and the wafer bottom is about 0.5 mils or less.
5. The wafer is then scribed with the well located at the center of each pellet.

The subsequent operations are similar to the ones outlined in the first report. The p-contact is placed at the bottom of the well. During the electrolytic etching to define the junction, the diffused p^+ region is removed from all areas of the wafer except under the p-contact. Some problems have been experienced in accurately placing the contact inside the well, and also in controlling the well depth to close tolerances. In general, however, this process appears to be much more reproducible than the one in which the whole pellet thickness is reduced. Results achieved to date are very encouraging. Figure (5) is a photographic cross section of a well etched prior to diffusion. The diffused junction is outlined.

Table II compares one lot of well units with a control lot of 2 mil pellets made from the same crystal. The particular crystal used was of a rather high resistivity (.07 ohm-cm), in order to make the base resistance an appreciable part of the total diode resistance. The improvement brought about by the use of the well technique is, therefore, clearly discernible. Table II shows that the well units are about three times better than the control lot.

FIGURE 5 CROSS SECTION OF ETCHED WELL IN GALLIUM ARSENIDE VAPOR SHOWING DIFFUSED p^+ REGION (150X)

TABLE II

EXPERIMENT COMPARING WELL PROCESS TO STANDARD

Well Units			Standard Units		
C_{jo} (pf)	V_B (volts)	f_c § (at V_B)	C_{jo} (pf)	V_B (volts)	f_c § (at V_B)
0.355	54	210	0.790	45	90
0.413	55	330	0.689	58	108
0.418	40	310	0.772	44	80
0.276	52	340	0.762	47	90

§Extrapolated from cutoff frequency measured at - 6 volts and 10kmc/s

The resistance of the base region of the control lot is estimated to be approximately 5 ohms. When other resistances are considered, the computed cutoff frequency at breakdown is about 125 kmc/s close to the average measured value of 90 kmc/s.

The well units have base thicknesses of about .4 mils. The total resistance is, therefore, about 3.5 ohms, and the computed cutoff frequency at breakdown is 400 kmc/s. The agreement with the average measured values of 320 kmc/s is again reasonably close.

2. Epitaxial Diodes

Work has continued this quarter on epitaxial diodes. N-type layer resistances in the range of 3×10^{16} cm^{-3} to 8×10^{16} cm^{-3} have been used. The breakdown voltages measured on these devices were generally lower than those achieved using non-epitaxial Gallium Arsenide with similar carrier concentration. The reverse characteristic of epitaxial diodes have been found to be highly variable. A number of the diodes fabricated on low resistivity layers (10^{17} cm^{-3}) were soft

while typical non-epitaxial diodes are hard. The softness of the curves is believed to be caused by the presence of crystal defects. Some devices made on higher resistivity epitaxial layers gave evidence of the presence of localized breakdown similar to the effects found in silicon (microplasmas). (K.G. McKay "Avalanche Breakdown in Silicon", Phys. Review, Vol. 94, p. 877, 1954).

Figure (6) is an oscilloscope photograph of the discontinuous reverse I-V characteristics in the breakdown region of such a diode. The bulk breakdown appears to occur at about 18 volts, but the useful voltage range is limited to 12 volts.

The cutoff frequencies measured on the two and three best devices were in the order of 300 kmc at breakdown, with breakdowns varying from 9 to 18 volts. These are still below the values which can theoretically be expected. The cause of very high resistances found in some of the epitaxial units is not yet determined.

C. Thermal Resistance

The thermal resistance of a group of non-epitaxial diodes have been tested to determine the allowable power dissipation level. The data is shown in Table III. The allowable power dissipation is given by:

$$P_{(max)} = \frac{T_{j\,(max)} - T_A}{R_{th}}$$

where:

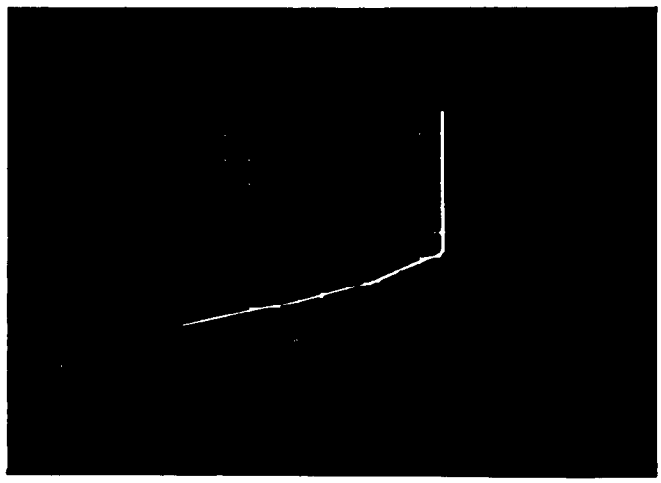
$T_{j\,(max)}$ = maximum allowable junction temperature

T_A = ambient temperature, and

R_{th} = thermal resistance of the device

$T_{j\,(max)}$ has been determined to be about 175°C. For T_A = 25°C the average calculated allowable power dissipation is in excess of one watt

2 MICROAMPERES/DIVISION



2 VOLTS/DIVISION

FIGURE 6 REVERSE I-V CHARACTERISTICS OF AN EPITAXIAL GALLIUM ARSENIDE DIODE SHOWING THE PRESENCE OF LOCALIZED BREAKDOWN (LAYER RESISTIVITY $\sim 5\text{x}10^{16}$)

per pf (zero bias) for the devices tested. This value assumes of course that an adequate heat sink is used.

Further measurements are being made on lower voltage diodes.

TABLE III

THERMAL RESISTANCE OF GALLIUM ARSENIDE DIODES

C_{jo} (pf)	V_B (volts)	Thermal Resistance °C/watt
0.813	51	90
1.060	63	91
0.764	58	91
0.765	82	112
0.604	76	102
0.850	37	94
0.637	60	146
0.449	55	148
0.805	68	161

D. Electrical Measurements

1. Capacitance

Careful measurements of capacitance as a function of reverse junction potential have been made at one mc on several epitaxial and non-epitaxial diodes. Figure (7) shows the capacitance-voltage characteristics of an epitaxial diode (V_B = 18 volts) and a non-epitaxial diode (V_B = 24 volts). The non-epitaxial diode shows a constant slope of 1/3, indicating a normal spread of the space charge region. The epitaxial diode, however, has a break in the slope of the curve at about 7 volts, indicating that the spread of the space charge region begins to slow down at that point. This in not surprising since the

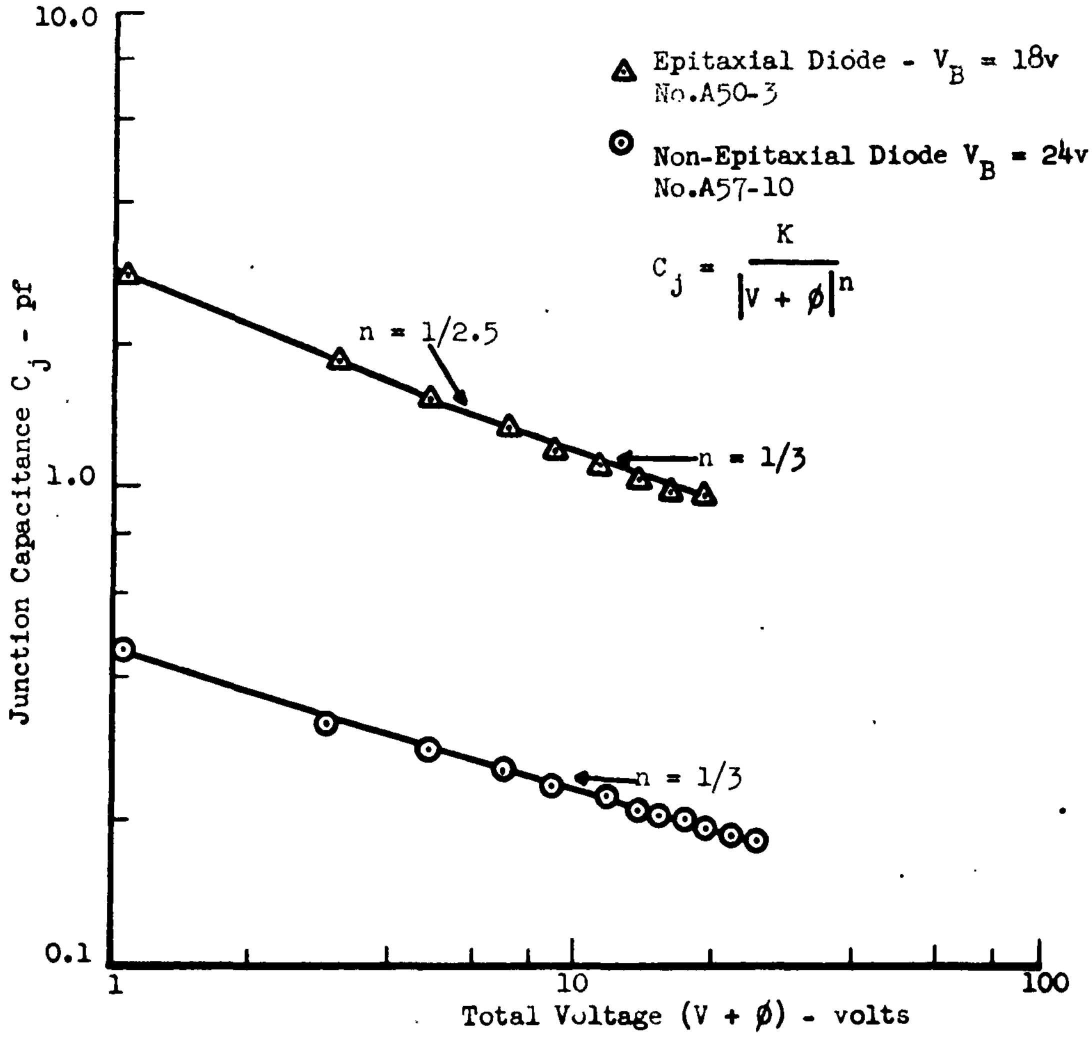


FIGURE 7 CAPACITANCE-VOLTAGE CURVE FOR AN EPITAXIAL DIODE AND NON-EPITAXIAL DIODE ASSUMING ϕ = 1 volt

epitaxial layers are known to be generally graded. The first part of the curve yields an n factor of 1/2.5, the remainder has a value of 1/3.

2. Cutoff Frequency

Cutoff frequency measurements are being made using the technique outlined in the first report. The ΔQ is presently being measured between 0 volts and -2 volts, rather than between -1 volt and -6 volts, to enhance the accuracy of the measurement for high Q diodes. No substantial difference between the two methods have been found to date. Figure (8) is a Smith Chart plot of a typical diode.

Diode No. 622-11: V_B = 13 volts, C_{jo} = 0.545, C_{j-2} = 0.386, f_{c-2} = 153 kmc/sec.

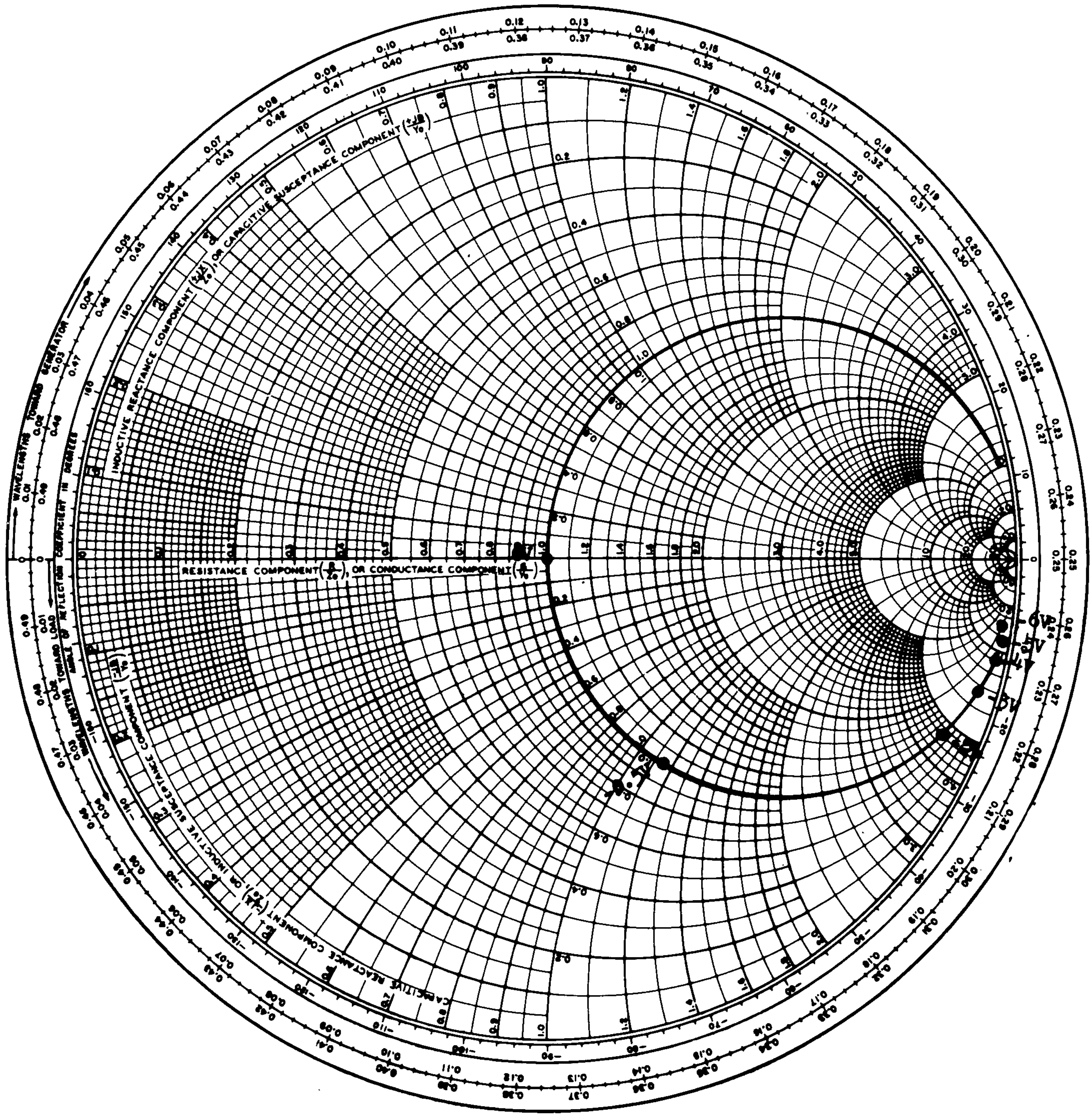


FIGURE 8 SMITH CHART PLOT OF A TYPICAL DIODE

III. CONCLUSIONS

Calculations, confirmed by experimental results, indicate that substantial improvements in series resistance may be achieved in non-epitaxial Gallium Arsenide diodes by using either thin structures or well structures. The second technique appears to be more reproducible. Continued work with epitaxial material indicates that the quality is still variable. While a small number of good devices were fabricated in the 8-18 volt range, they were not generally superior to the non-epitaxial units and were produced with a small yield.

Thermal resistance measurements indicate that the allowable power dissipation with adequate heat sinks for devices fabricated using 0.07 - 0.09 ohm-cm material is in excess of one watt per pf junction capacitance at zero bias.

The calculated characteristics required to meet the goals of Phase II of the contract have been met or exceeded by a number of the devices fabricated during this reporting period.

PART II

I. PROGRAM FOR NEXT PERIOD

(A) Continued improvements in device structure to improve cutoff frequencies of devices with breakdown voltages in excess of 20 volts.

(B) Further investigations of the properties of epitaxial diodes to determine the cause of the present limitations.

(C) Improvements in device contacts to reduce series resistance.

(D) Further measurements of thermal resistance of devices.